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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/017,806	10/30/2001	Ming-Yu Lin	JCLA7567	5265

7590 05/04/2004

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EXAMINER	
CROSS, LATOYA I	
ART UNIT	**PAPER NUMBER**
1743	

DATE MAILED: 05/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/017,806	LIN ET AL.	
	Examiner	Art Unit	
	LaToya I. Cross	1743	eh

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 30 October 2001.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-9 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-9 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 30 October 2001 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Observations

- Claim 9 depends from claim 1 and recites "before the step of transporting the wafer to the main etch chamber". There is insufficient antecedent basis for this limitation. It is suggested that Applicants amend claim 9 to be dependent on claim 8.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 3 and 8 are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent 5,868,853 to Chen et al (hereinafter Chen et al '853).

Chen et al '853 teach a method for cleaning a process chamber after an etching process is conducting. Chen et al '853 teach that in a silicon nitride etching process, a wafer is coated with a photoresist layer, patterned and placed in an etch chamber (col. 2, lines 35-57). In a comparison example, Chen et al '853 teach that after the etching process takes place, the wafer

is removed from the chamber and the number of contaminating particles on the wafer is counted (col. 6, lines 34-43). See also Table 2. Chen et al '853 teach that the presence of contamination particles in a process chamber during etching leads to the formation of voids, dislocations or short-circuits resulting in performance and reliability problems, and in reduction in yield. In counting the number of particles on the wafer after the etching process, one can determine the cleanliness of the process chamber (col. 1, lines 14-39). With respect to claim 8, Chen et al '853 teach a wafer (30) is disposed in etcher (10) having an etching chamber (20). The reference further teaches that etcher (10) is a plasma etching chamber for conducting a plasma etching process (col. 1, line 65 – col. 2, line 16).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claims 2 and 4-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al '853 in view of US Patent 6,699,399 to Qian et al.

The disclosure of Chen et al '853 is described above. With respect to claim 2, Chen et al '853 differ from the instantly claimed invention in that there is no disclosure of the duration of time for which the etching process takes place. With respect to claims 4-7, Chen et al '853 teaches counting contaminating particles in silicon nitride etching processes; however, the reference fails to teach silicon oxide, polysilicon and metal etching processes.

With respect to the duration of time for the etching process, Chen et al '853 teaches that an etching process (over etching) takes place for approximately 20-25 seconds. It is the position of the Examiner that the teaching of Chen et al '853 of "approximately 20 seconds" is sufficient to read on Applicants' recitation of 15 seconds, absent evidence of unexpected results in using 15 seconds or less.

With respect to etching processes other than silicon nitride etching, Qian et al teaches that in manufacturing integrated circuit devices, silicon dioxide, silicon nitride, polysilicon, metal silicide and monocrystalline silicon on a substrate undergo etching processes including the forming of a photoresist layer on the substrate. The reference further teaches that during all of these etching processes, residues from the process are deposited on the walls of the processing chamber, which may lead to unwanted contamination of the substrate, itself.

While Chen et al '853 discloses counting contaminating particles resulting from silicon nitride etching processes, it would have been obvious to one of ordinary skill in the art to determine the number of particles resulting from other etching processes (including polysilicon, silicon dioxide and metal) to determine the cleanliness of these processing chambers since Qian et al teach that contaminating particles result from all of these processes. In determining the number of contaminating particles in all processes, the use would be notified of when the

processing chamber should be cleaned and counting the contaminates would indicate the possibility of contaminated wafers being produced.

7. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chen et al '853 in view of US Patent 4,341,582 to Kohman et al.

With respect to claim 9, Chen et al '853 differs from the instantly claimed invention in that there is no disclosure of a port, vacuum chamber and alignment chamber.

Kohman et al teach that a common problem with etching wafers is atmospheric contamination of the photoresist coating, which results in undesirable effects. Kohman et al teach that pretreating the wafer in a vacuum overcomes this problem by preventing the wafer from being exposed to the atmosphere before the etching process. See col. 1, lines 47-56. Kohman et al also teach using a prealignment stage (16) in the etching process to align the wafer in its correct position before entering the etching chamber.

It would have been obvious to one of ordinary skill in the art to transport the wafers of Chen et al '853 to a vacuum chamber to prevent any external contamination from the outside environment. Further, it would have been obvious to transfer the wafer to a pre-alignment chamber to aid in aligning the wafer in the correct position and prepare the wafer for etching.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to LaToya I. Cross whose telephone number is 571-272-1256. The examiner can normally be reached on Monday-Friday 8:30 a.m. - 5:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jill A. Warden can be reached on 571-272-1267. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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